VPX599

Dual DAC 12 GSPS, Dual ADC 6.4 GSPS, Kintex UltraScale™, 3U VPX

VPX599

Key Features

- 3U FPGA Dual DAC and dual ADC per VITA-46
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC @ 6.4 GSPS 12-bits
- Dual DAC @ 12 GSPS 16-bits (AD9162 or AD9164)
- High-performance clock jitter cleaner
- VHDL reference design with source code
- Protocols such as PCIe, SRIO, 10GbE/40GbE, etc. are FPGA programmable
- 16 GB of DDR-4 Memory (64-bit wide)

Applications

- RADAR data processing
- SIGINT/EW
- Command and Control

OpenVPX™

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The VPX599 provides dual-channel ADC with sample rates of up to 6.4 GSPS at 12-bits and a dual DAC update rate of up to 12 GSPS and direct RF synthesis at 6 GSPS at 16-bits making it suitable for signal capture/analysis applications such as COMINT/SIGINT, radar, research and instrumentation.

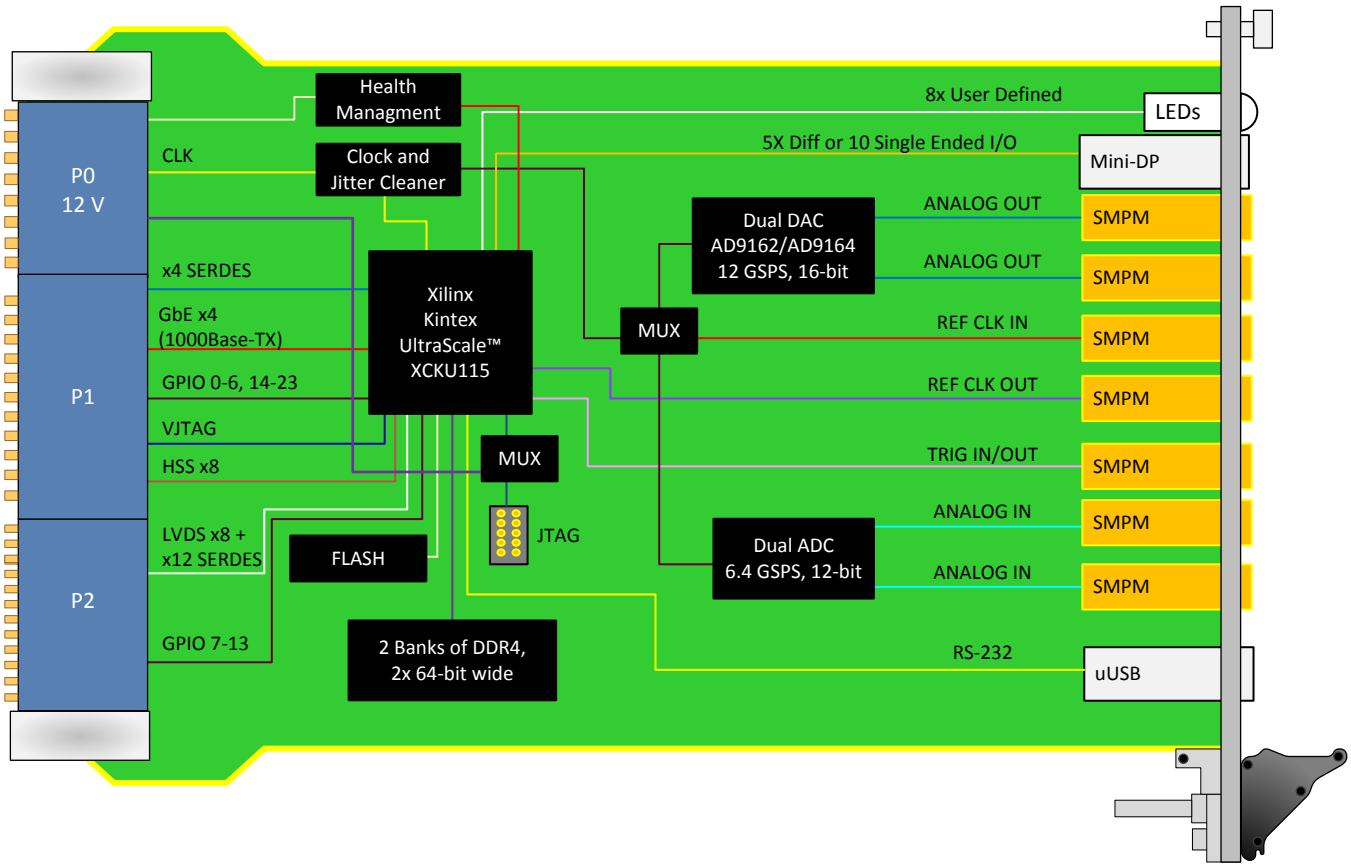
The unit has an on-board Kintex UltraScale™ XCKU115 FPGA which interfaces directly to ADC/DAC. The FPGA has interface to two banks of 64-bit wide DDR4 memory channels with a total of 16 GB memory.

The module routes to the P1/P2 connectors Quad GbE, x16 high speed SERDES that could be configured as PCIe/SRIO/40GbE/10GbE/Aurora, GPIO, etc. The module has an on board dedicated health management CPU which complies with the OpenVPX standard.

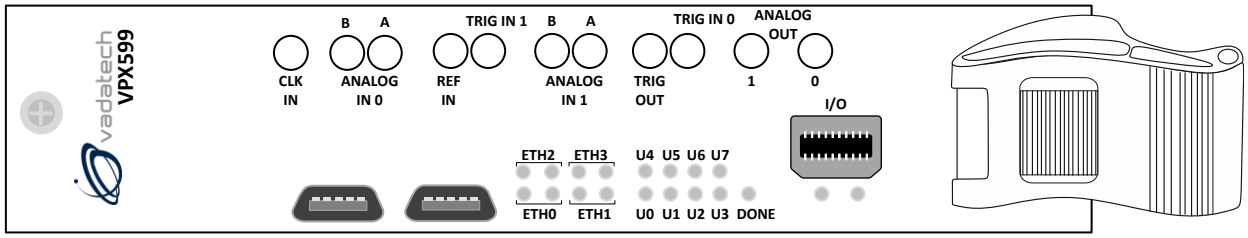
The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA-47, up to V3 and OS2.

Please contact VadaTech for details of Conduction Cooled versions.

Block Diagram



Front Panel



Xilinx Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tool for developing Digital Signal Processing (DSP) applications.

Xilinx Vivado Design Suite, Xilinx System Generator for DSP

Specifications

Architecture		
Physical	**Dimensions**	3U, 1" pitch
FPGA		Xilinx Kintex UltraScale™ XCKU115
Configuration		
Power		~40 W (dependent on FPGA load), could be as high as 60W
Memory		Two banks of DDR4, 64-bit wide (16 GB total)
Front Panel	**SMPM**	Dual Analog In, dual Analog Out, Trig In/Out and Ref Clock In
	Micro USB	RS-232 from Health Management CPU
		RS-232 from FPGA
	LEDs	User defined by the FPGA and Health Management
On-board Interfaces		None
VPX Interfaces	**Slot Profiles**	See ordering options
	Rear IO	x4 high speed serial links on P1 (PCIe, 10GbE/40GbE/ SRIO/Aurora per FPGA load)
		x12 high speed serial links on P2 (PCIe, 10GbE/40GbE/SRIO/Aurora per FPGA load)
		x4 GbE on P1 as 1000Base-TX
		x23 GPIO
		JTAG
	Power Supplies	On P0: VS1 = 12 V
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of ATCA and µTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTM), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX599– AB0-DEF-GHJ

A = RF Direct Clock Sampling	D = FPGA Speed	G = Applicable Slot Profiles
0 = Front Panel 1 = On-board wide band PLL	0 = Reserved 1 = High 2 = Highest	0 = 5 HP
B = DAC	**E = Clock Holdover Stability**	**H = Environmental**
0 = AD9162 1 = AD9164	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification table option H description
	F = PCIe Option (P1)	**J = Conformal Coating**
	0 = None (40GbE, 10GbE, SRIO, etc.) 1 = PCIe x4	0 = None 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H=4**
Operating Temperature	AC1* (0°C to +55°C	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

* Nomenclature per ANSI / VITA-47

Related Products

VPX516

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA-46 and VITA-57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX517

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA-46 and VITA-57
- Xilinx Kintex-7 410T FPGA in FFG-900 package
- High-performance clock jitter cleaner

VPX592

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA-46 and VITA-57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014

Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan

Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

info@vadatech.com | www.vadatech.com

Europe: EMCOMO Solutions AG

Industriestr. 10, 89231 Neu-Ulm, Germany

Phone: +49 731 8803510 | Fax: +49 731 88035129

vadatech@emcomo.de | www.emcomo.de

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